Application Note 1799

Author: Manjing Xie

ISL9444EVAL3Z: Triple PWM Step-Down Synchronous Converters

Introduction

ISL9444EVAL3Z consists of three PWM step-down synchronous converters, which features the triple PWM controller, ISL9444. The PWM1 delivers 5V output at 5A. PWM2 and PWM3 deliver 5V at 25A and 3.3V at 25A, respectively.

A power failure monitor and three independent enable pins accommodate variable power sequencing requirement. The Extbias option is provided to achieve low standby power.

Strong gate driver and adaptive deadtime control achieve excellent efficiency over 96%.

ISL9444 Key Features

- Wide input voltage range: 4.5V to 28V
- Use lower MOSFET's $r_{DS(ON)}$ for current sensing
- Extbias pin to save operating loss
- Power failure monitor
- Complete protection: overvoltage, overcurrent, thermal shutdown
- Three independent power-good indicators

Evaluation Board Specifications

TABLE 1. EVALUATION BOARD ELECTRICAL SPECIFICATIONS

SPEC	DESCRIPTION	MIN	TYP	MAX	UNIT
VIN	Input for PWM2 and PWM3	5.6	12	16	V
VOUT2	IOUT = 0A	4.75	5.0	5.25	V
VOUT3	IOUT = 0A	3.15	3.3	3.65	V
IOUT_2 IOUT_3	Output Current of PWM2 and PWM3	25			A
VIN2	Input for PWM1	5.6	12	16	V
VOUT1	IOUT = 0A	4.75	5	5.25	V
IOUT_1	Output Current of PWM1	6			A
F_{SW}			330		kHz
η	VIN = 12V, PWM1, 6A, EN2 = EN3 = GND		96		%
η	VIN = 12V, PWM1 at 6A, PWM 2 and PWM3 at 25A respectively		95.9		%

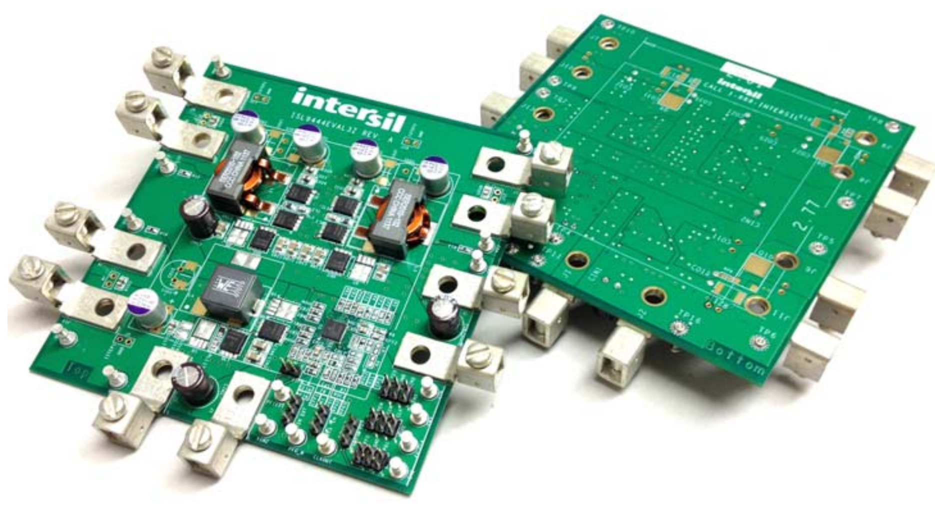


FIGURE 1. ISL9444EVAL3Z TOP AND BOTTOM VIEW

TABLE 2. RECOMMENDED COMPONENT SELECTION FOR QUICK EVALUATION FOR PWM CHANNEL

V_{OUT} (V)	I_{OUT} (A)	V_{IN} (V)	F_{SW}(kHz) /R_T(kΩ)	MOSFET(s), LOWER, UPPER	RSEN	INDUCTOR (L, ISAT)	COUTs	FEEDBACK RES (LOWER, UPPER, kΩ)	CFF
12	15	19 to 26.4	250/130	1XBSC059N04, 1XBSC059N04	2.0kΩ	4.7µH, 20A	270µF, OSCON, 16V and 2x1.0µF, ceramic	3.24, 52.3	1nF

NOTES:

1. Please select the output capacitor with a voltage rating higher than the output.
2. Please adjust R_{OCSET} accordingly.
3. Please contact Intersil Sales for assistance.

Recommended Equipment

The following equipment is recommended for evaluation:

- 0V to 20V power supply with 30A source current capability
- Electronic load capable of sinking 30A @ 20V
- Digital Multimeters (DMMs)
- 100MHz Quad-Trace Oscilloscope

Quick Test Setup

1. Ensure that the evaluation board is correctly connected to the power supply and the electronic load prior to applying any power. Please refer to Figure 2 for proper set-up.
2. Refer to Table 3 for jumper default positions. For set-up different than the default setting, please refer to the datasheet for details (ISL9444, FN7665).
3. Turn on the power supplies; V_{IN} < 16V; V_{IN2} < 16V
4. Adjust input voltage V_{IN} and V_{IN2} within the specified range and observe output voltage. The output voltage variation should be within 5%.
5. Adjust load current within specified range. The output voltage variation should be within 5%.
6. Use an oscilloscope to observe the output ripple voltage and phase node ringing. For accurate measurement, please refer to Figure 3 for proper probe set-up.
7. Optimization. Please refer to Table 2 on page 1 for optimization recommendation.

NOTE: All Test points are for voltage measurement or small signal only. Do not allow high current through these test points.

TABLE 3. JUMPER DEFAULT POSITIONS

JUMPER NAME	PFI	EN1	EN2	EN3	MODE
Positions	VIN	EN	PFO	EN2	CCM

Probe Set-up

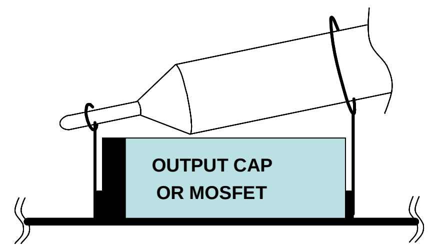


FIGURE 3. OSCILLOSCOPE PROBE SET-UP

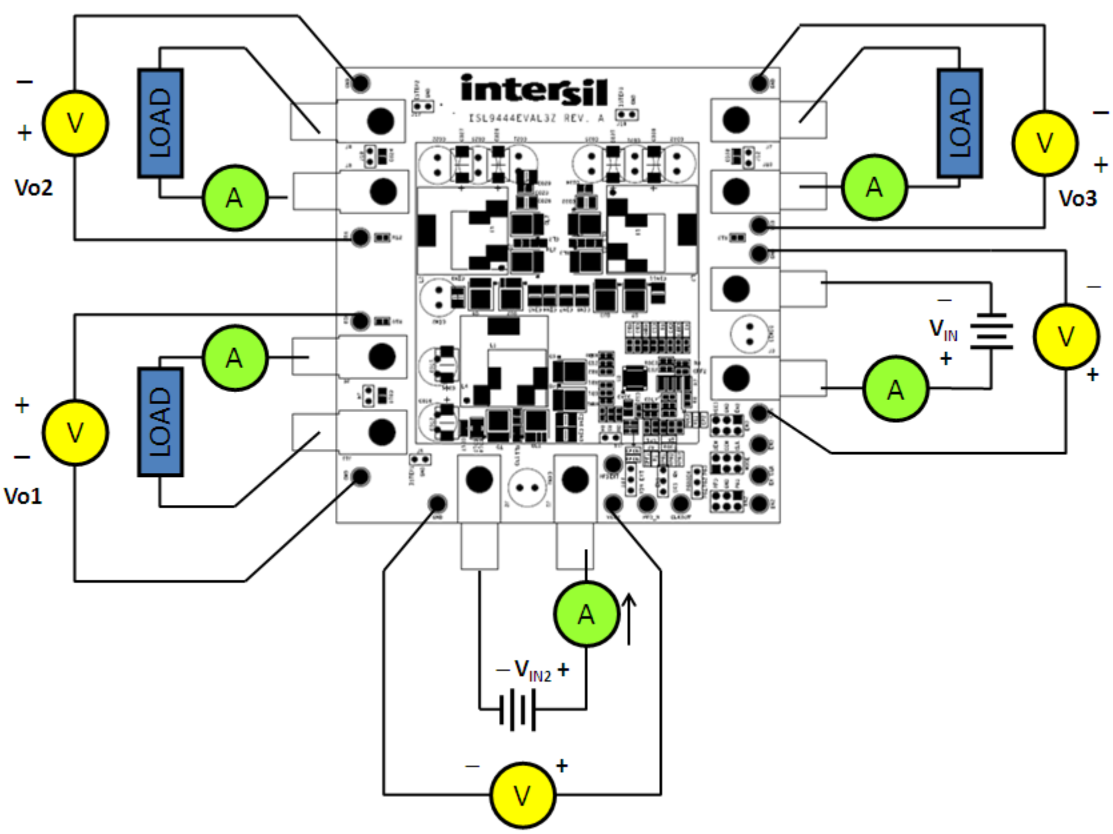


FIGURE 2. ISL9444EVAL3Z TEST SET-UP

Output Setting

The output voltage is set by the feedback resistor divider, R_{low} and R_{up}.

$$V_{OUT} = \frac{R_{low} + R_{up}}{R_{low}} \times 0.7V \quad \text{(EQ. 1)}$$

Where R_{low} is the resistor from FBx to GND, R_{up} is the resistor from VOx to FBx. Resistor R10, R12 and R13 are resistor jumpers for loop gain measurement. They are not must-to-have components. It is recommended to use 50Ω for loop gain measurement.

Remote Sensing

By sensing the positive rail from load, significant voltage drop along the PCB trace can be compensated.

For applications with load far from the ISL9444, it is likely that the remote sensing trace picks up noise from the environment. To prevent noise being coupled into the feedback loop, it is recommended to connect the phase boosting capacitors, C_{ff1}, C_{ff2} and C_{ff3} to the local output capacitors.

For applications that C_{ffx} is not used for phase boosting, a pair of C_{ff} and C_p is recommended for remote sensing. Please set C_{ff} and C_p according to Equation 2.

$$R_{low} \cdot C_P = R_{up} \cdot C_{ff} \quad \text{(EQ. 2)}$$

In case the remote sensing trace become open-circuit, a default resistor is recommended to connect the resistor R_{up} to the local VOUT.

The ISL9444 does not provide dedicated differential amplifier for remote sensing.

Transient Load Test

The ISL9444EVAL3Z provides optional load transient test footprints for high di/dt load transient response tests. Please refer to Figure 4 for the load transient circuit of PWM1.

1. Select a powerpak or SOIC8 MOSFET with VDSS breakdown greater than VOUT. Select a current sensing resistor. For accurate current sensing, please use tighter than 5% tolerance resistors. To alleviate thermal stress, use 0.1Ω or smaller resistance. For 25A application, a 10mΩ precision resistor is recommended. Use an oscilloscope to monitor voltage across R21 and the output voltage.
2. Install the load transient circuit as indicated in the "Schematic (Optional Circuits and Optional Footprints)" on page 8. R18, R20 and R22 are 10kΩ resistors for MOSFET gate discharging.
3. Apply pulse square waveform to the gate of the load transient test MOSFET, Q10. The duty cycle of the pulse waveform should be small (<5%) to limit thermal stress on current sensing resistor and the MOSFETs. Set the amplitude of the square waveform below 0.5V at the beginning.
4. The amplitude of the square waveform set the current step amplitude. Slowly increase the amplitude of the square waveform and monitor the current amplitude. Adjust the square waveform rising and falling time to set the current step slew rate.
5. Monitor overshoot and undershoot at the corresponding output.

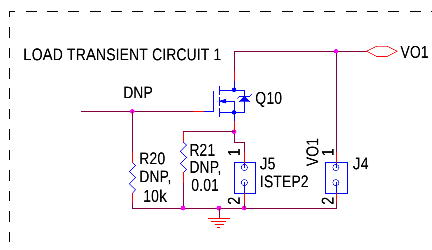


FIGURE 4. LOAD TRANSIENT SET-UP

Typical Performance Curves

Oscilloscope Plots were taken at V_{IN} = 12V, V_{IN2} = 12V and jumpers in default positions, unless otherwise noted.

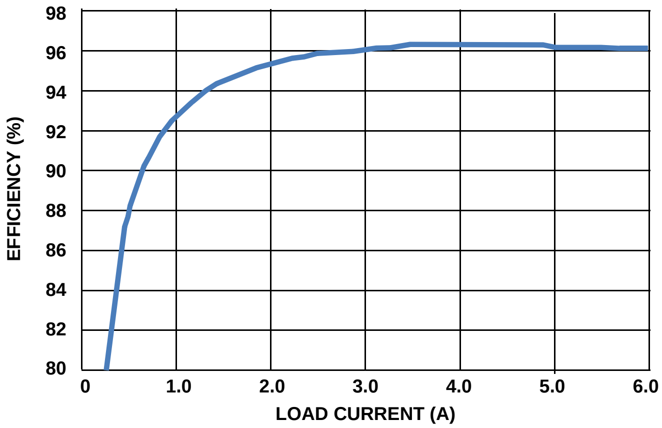


FIGURE 5. EFFICIENCY vs LOAD CURRENT FOR PWM1 (EN2 = EN3 = GND)

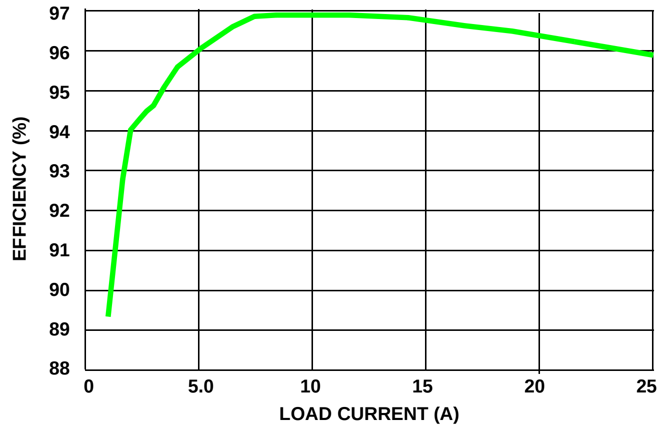


FIGURE 6. TOTAL EFFICIENCY vs LOAD PWM2 AND PWM3 (EN/SS1 IS GROUNDED)

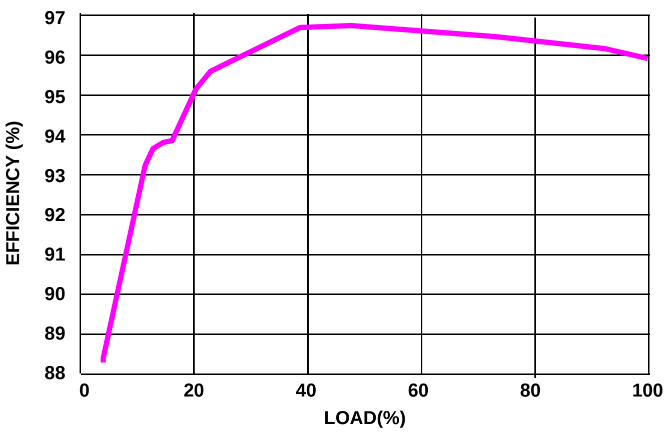


FIGURE 7. EFFICIENCY vs LOAD(%) FOR ALL PWMs (6A, 25A, 25A)

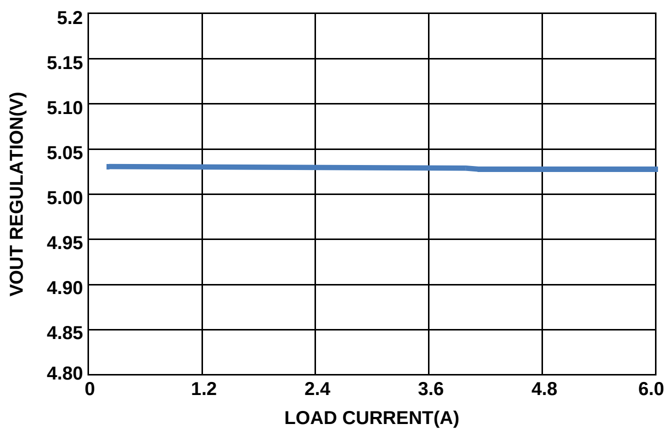


FIGURE 8. LOAD REGULATION OF PWM1 (V_{IN2} = 12V)

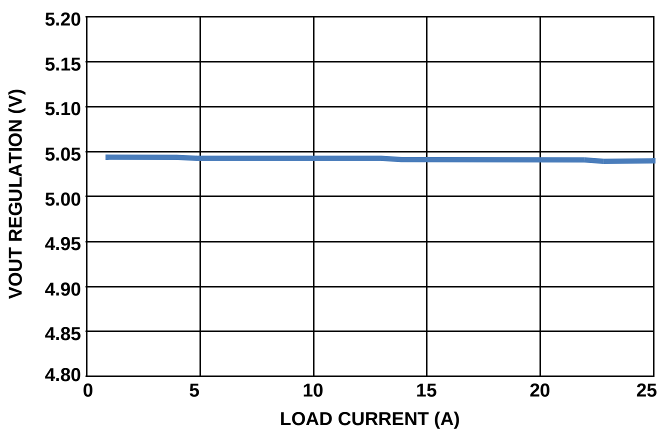


FIGURE 9. LOAD REGULATION of PWM2 (V_{IN} = 12V)

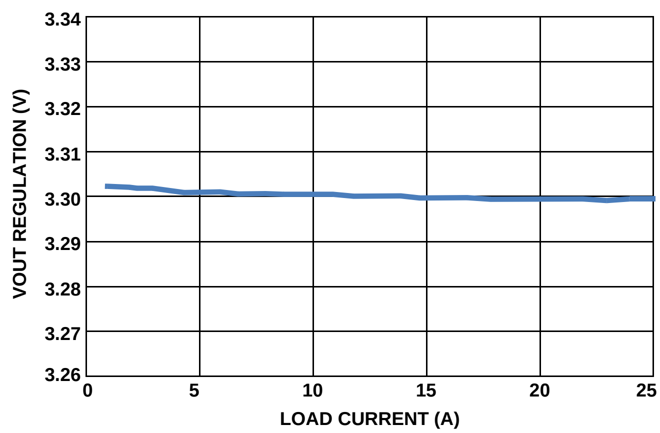


FIGURE 10. LOAD REGULATION of PWM3 (V_{IN} = 12V)

Typical Performance Curves

Oscilloscope Plots were taken at V_{IN} = 12V, V_{IN2} = 12V and jumpers in default positions, unless otherwise noted. **(Continued)**

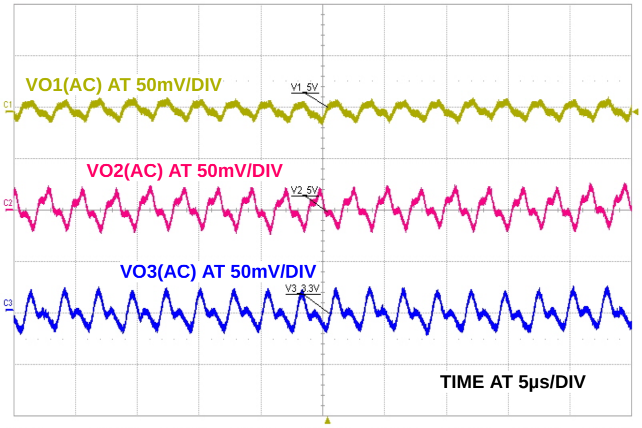


FIGURE 11. OUTPUT RIPPLE (V_{IN} = 12V, FULL LOAD, 20MHz BW)

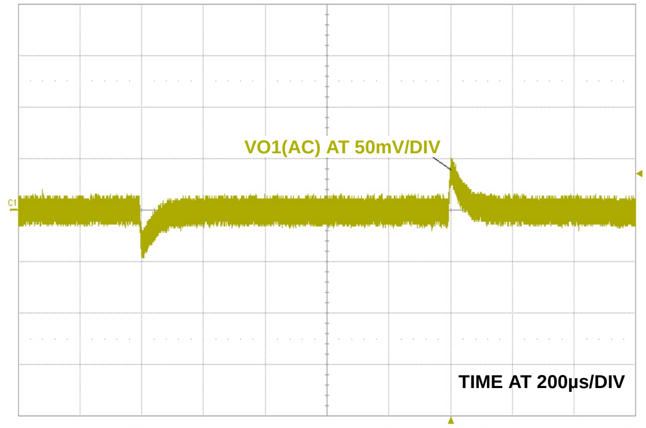


FIGURE 12. LOAD TRANSIENT RESPONSE of PWM1 (1.25A TO 3.75A AT 2A/µs)

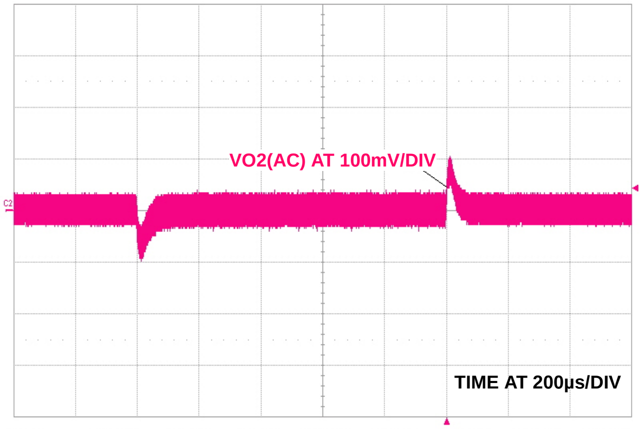


FIGURE 13. LOAD TRANSIENT RESPONSE of PWM2 (6.25A TO 18.75A AT 2A/µs)

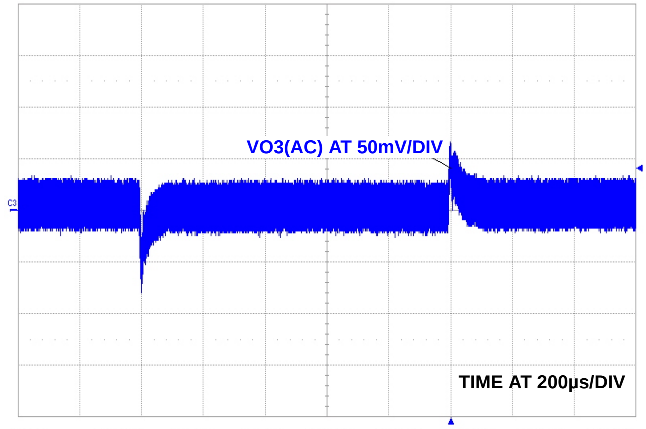


FIGURE 14. LOAD TRANSIENT RESPONSE OF PWM1 (6.25A TO 18.75A AT 2A/µs)

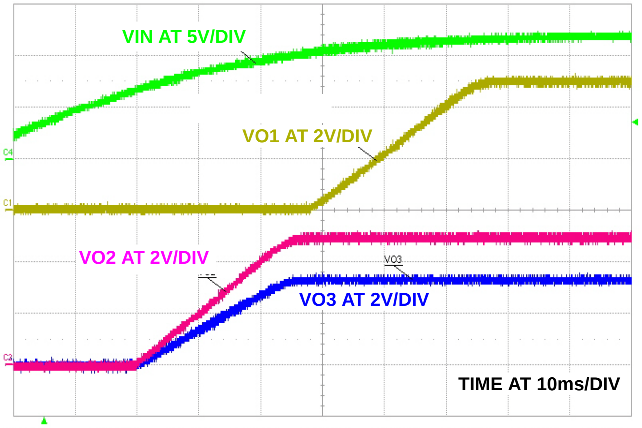


FIGURE 15. POWER-UP SEQUENCING (DEFAULT CONFIGURATION)

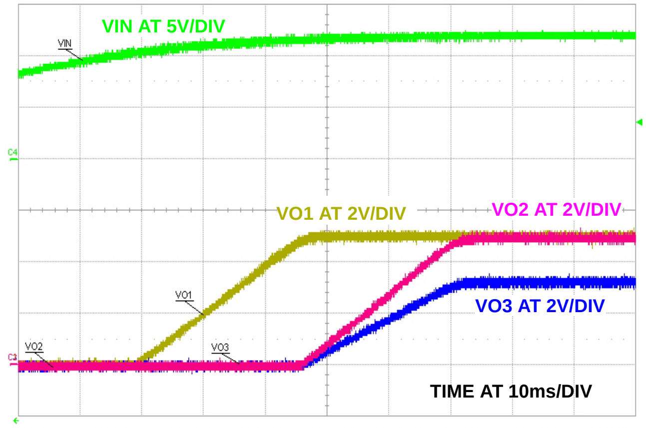


FIGURE 16. POWER-UP SEQUENCING (EN2 = PGOOD1)

Typical Performance Curves

Oscilloscope Plots were taken at V_{IN} = 12V, V_{IN2} = 12V and jumpers in default positions, unless otherwise noted. **(Continued)**

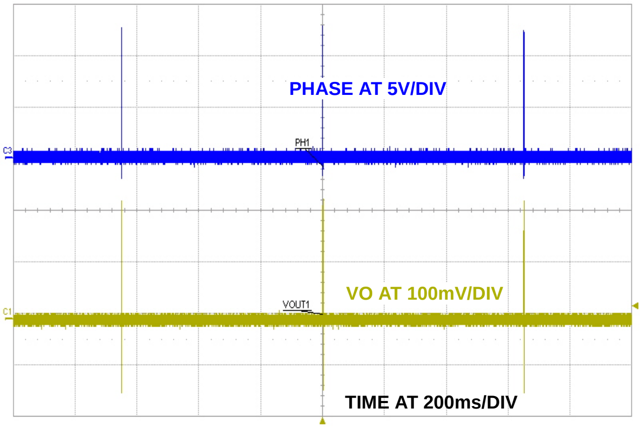


FIGURE 17. OVERCURRENT PROTECTION RESPONSE OF PWM1

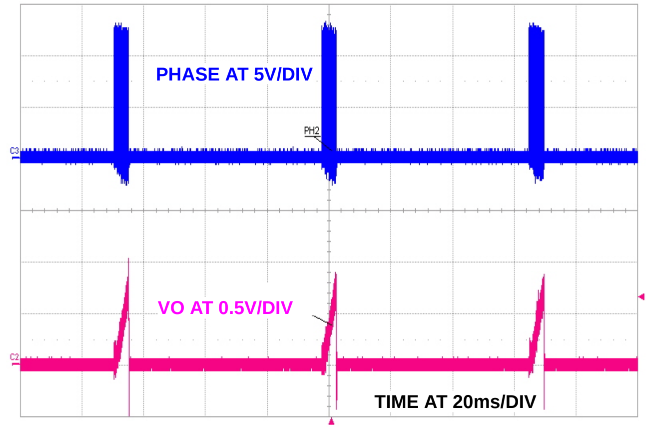
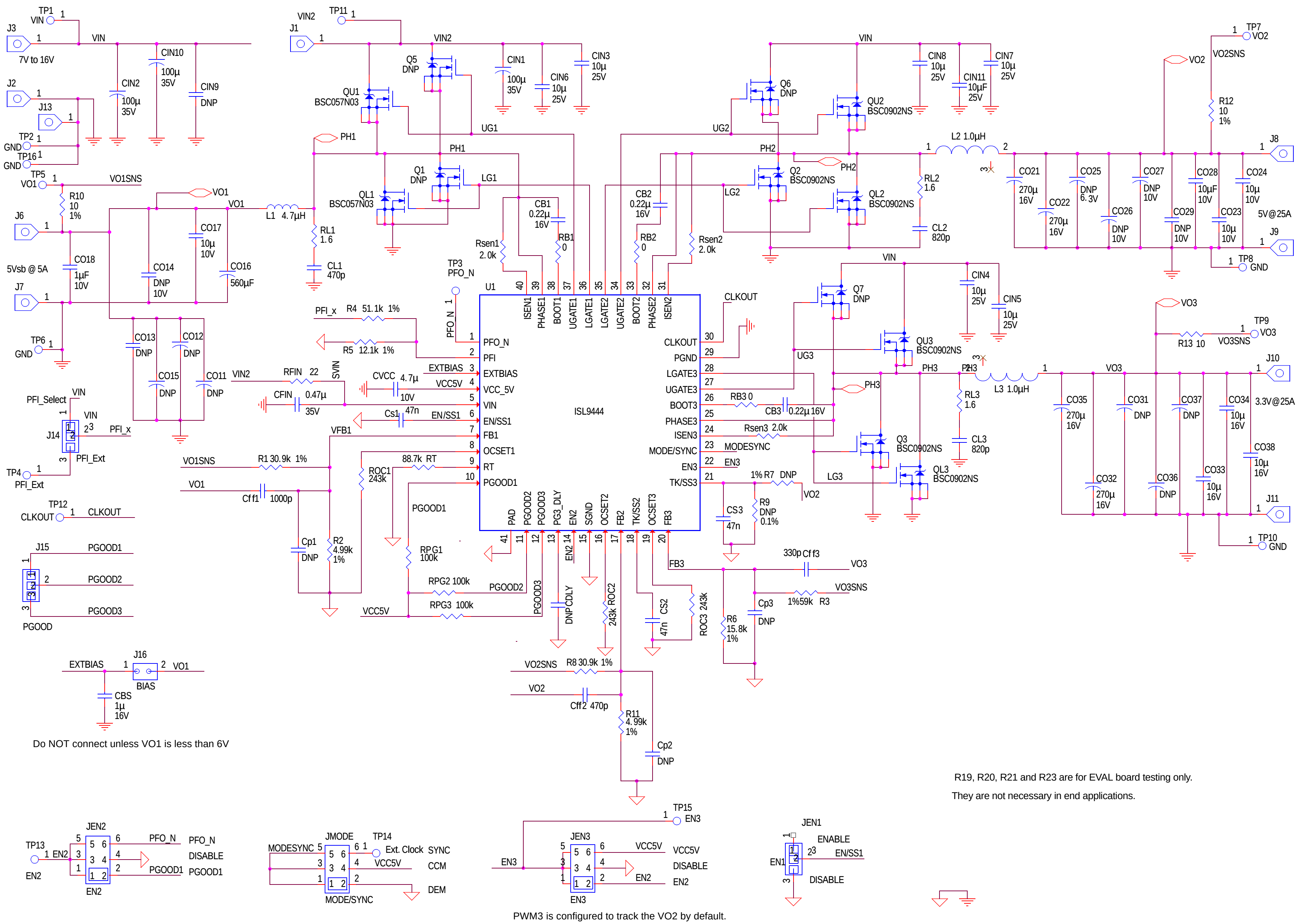
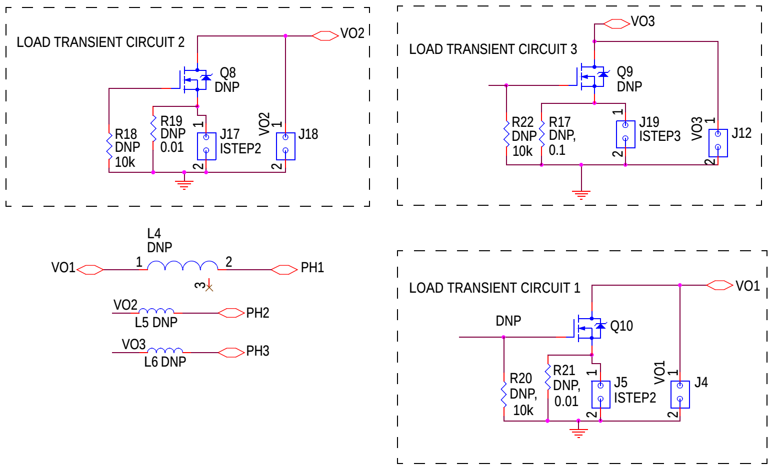


FIGURE 18. OVERCURRENT PROTECTION OF PWM2

Schematic, Main



Schematic (Optional Circuits and Optional Footprints)



Bill of Materials

ITEM	QTY	REFERENCE	VALUE	DESCRIPTION	PART #	VENDOR
ESSENTIAL COMPONENTS						
1	1	CBS	1µ	Ceramic CAP, X5R, 16V, SM0603	Generic	Generic
2	3	CB1, CB2, CB3	0.22µ	Ceramic CAP, X5R, 16V, SM0603	Generic	Generic
3	1	CFIN	0.47µ	Ceramic CAP, X5R, 35V, SM0603	Generic	Generic
4	3	CIN1, CIN2, CIN10	100µ	Alum. CAP, 25V	UTT1E101MPD	Nichicon
5	7	CIN3, CIN4, CIN5, CIN6, CIN7, CIN8, CIN11	10µ	Ceramic CAP, X5R, 25V, SM1206	Generic	Generic
6	1	CL1	470p	Ceramic CAP, NPO or COG, SM0805	Generic	Generic
7	2	CL2, CL3	820p	Ceramic CAP, NPO or COG, SM0805	Generic	Generic
8	8	CO17, CO18, CO23, CO24, CO28, CO33, CO34, CO38	10µ	Ceramic CAP, X5R, 10V, SM0805	Generic	Generic
9	5	CO16, CO21, CO22, CO32, CO35	270µF	OSCON, 16V, RADIAL 8x8	16SEPC270MX	SANYO
10	3	CS1, CS2, CS3	47n	Ceramic CAP, NPO or COG, SM0603	Generic	Generic
11	1	CVCC	4.7µ	Ceramic CAP, X5R 10V, SM0805	Generic	Generic
12	2	Cff1	1000p	Ceramic CAP, NPO or COG, SM0603	Generic	Generic
13	1	Cff2	470p	Ceramic CAP, NPO or COG, SM0603	Generic	Generic
14	1	Cff3	330p	Ceramic CAP, NPO or COG, SM0604	Generic	Generic
15	1	L1	4.7µH	INDUCTOR, ISAT > 10A	7443320470	Wurth Electronics
16	2	L2, L3	1.0µH	INDUCTOR, ISAT > 35A	SER2010-102ML	Coilcraft
17	2	QU1, QL1		Single Channel NFET, 30V	BSC057N03	Infineon
18	6	QU2, QL2, Q2, QU3, QL3, Q3		Single Channel NFET, 30V	BSC0902NS	Infineon
19	3	RB1, RB2, RB3	0	RESISTOR, SM0603	Generic	Generic
20	1	RFIN	22	RESISTOR, SM0603, 10%	Generic	Generic
21	3	RL1, RL2, RL3	1.6	RESISTOR, SM0805, 10%	Generic	Generic
22	3	ROC1, ROC2, ROC3	243k	RESISTOR, SM0603, 1%	Generic	Generic
23	3	RPG1, RPG2, RPG3	100k	RESISTOR, SM0603, 10%	Generic	Generic

Bill of Materials (Continued)

ITEM	QTY	REFERENCE	VALUE	DESCRIPTION	PART #	VENDOR
24	1	RT	88.7k	RESISTOR, SM0603, 1%	Generic	Generic
25	3	Rsen1, Rsen2, Rsen3	2.0k	RESISTOR, SM0603, 1%	Generic	Generic
26	2	R1, R8	30.9k	RESISTOR, SM0603,1%	Generic	Generic
27	2	R2, R11	4.99k	RESISTOR, SM0603,1%	Generic	Generic
28	1	R3	59k	RESISTOR, SM0603,1%	Generic	Generic
29	1	R4	51.1k	RESISTOR, SM0603, 1%	Generic	Generic
30	1	R5	12.1k	RESISTOR, SM0603,1%	Generic	Generic
31	1	R6	15.8k	RESISTOR, SM0603, 1%	Generic	Generic
32	3	R10, R12, R13	10	RESISTOR, SM0603, 10%	Generic	Generic
33	1	U1		Triple PWM Controller, 40L- 5x5 QFN	ISL9444IRZ	Intersil
EVAL BOARD HARDWARE AND RESISTOR JUMPERs						
34	3	JEN1, J14, J15		1x3 Header	Generic	Generic
35	3	JEN2, JEN3, JMODE		2x3 Header	Generic	Generic
36	10	J1, J2, J3, J6, J7, J8, J9, J10, J11, J13		CONN- Big Lug, TERMINAL POST	KPA8CTP	
37	1	J16	BIAS	1x2 Header	Generic	Generic
38	16	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16		CONN-TURRET, TERMINAL POST, TH	1514-2	KEYSTONE
39	5	JEN1, J14, JEN2, JEN3, JMODE		Connector Jumper	SPC02SYAN	Sullins
OPTIONAL FOOTPRINTs						
40	4	Cp1, Cp2, Cp3, CDLY	DNP	Ceramic CAP, NP0 or C0G, SM0603		
41	2	CO25, CO11, CO31	DNP	ELEC. CAP, RADIAL 8x8		
42	2	CO13, CO29, CO14	DNP	CAP, SM1210		
43	4	CO12, CO15, CO26, CO27, CO36, CO37	DNP	ELEC. CAP, SM7343		
44	6	J4, J5, J12, J17, J18, J19	DNP			
45	3	L4, L5, L6	DNP	INDUCTOR		
46	2	Q1, Q5, Q6, Q7	DNP	Single Channel NFET		
47	2	R7, R9	DNP	RESISTOR, SM0603		
COMPONENTs FOR LOAD TRANSIENT TEST CIRCUITs						
48	3	Q8, Q9, Q10	DNP	N-Channel MOSFET, TO252		
49	1	R17, R19, R21	DNP, 0.01	RESISTOR, SM2512		
50	3	R18, R20, R22	DNP, 10k	RESISTOR, SM0603		

ISL9444EVAL3Z PCB Layout

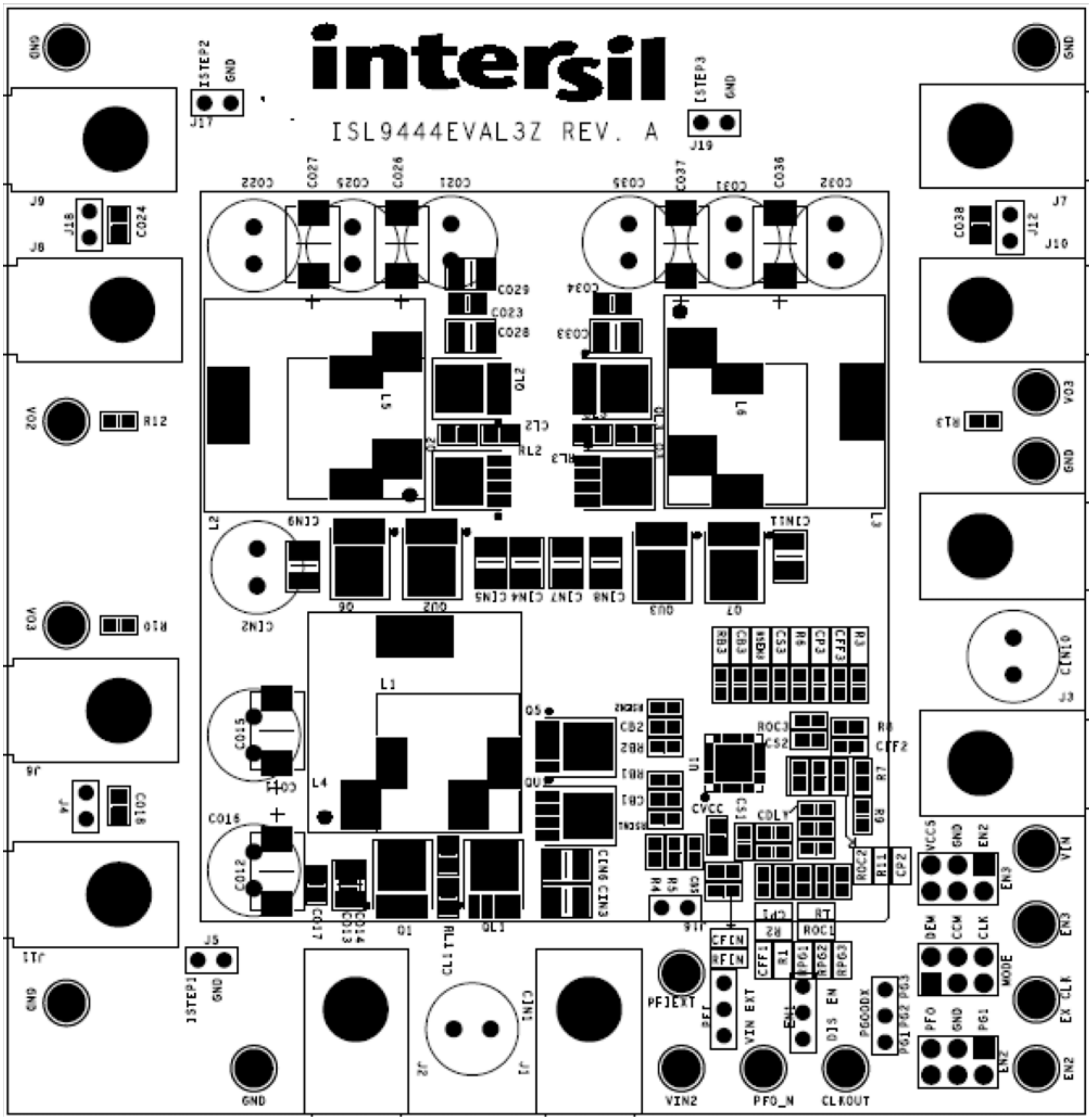


FIGURE 19. TOP SILKSCREEN

ISL9444EVAL3Z PCB Layout (Continued)

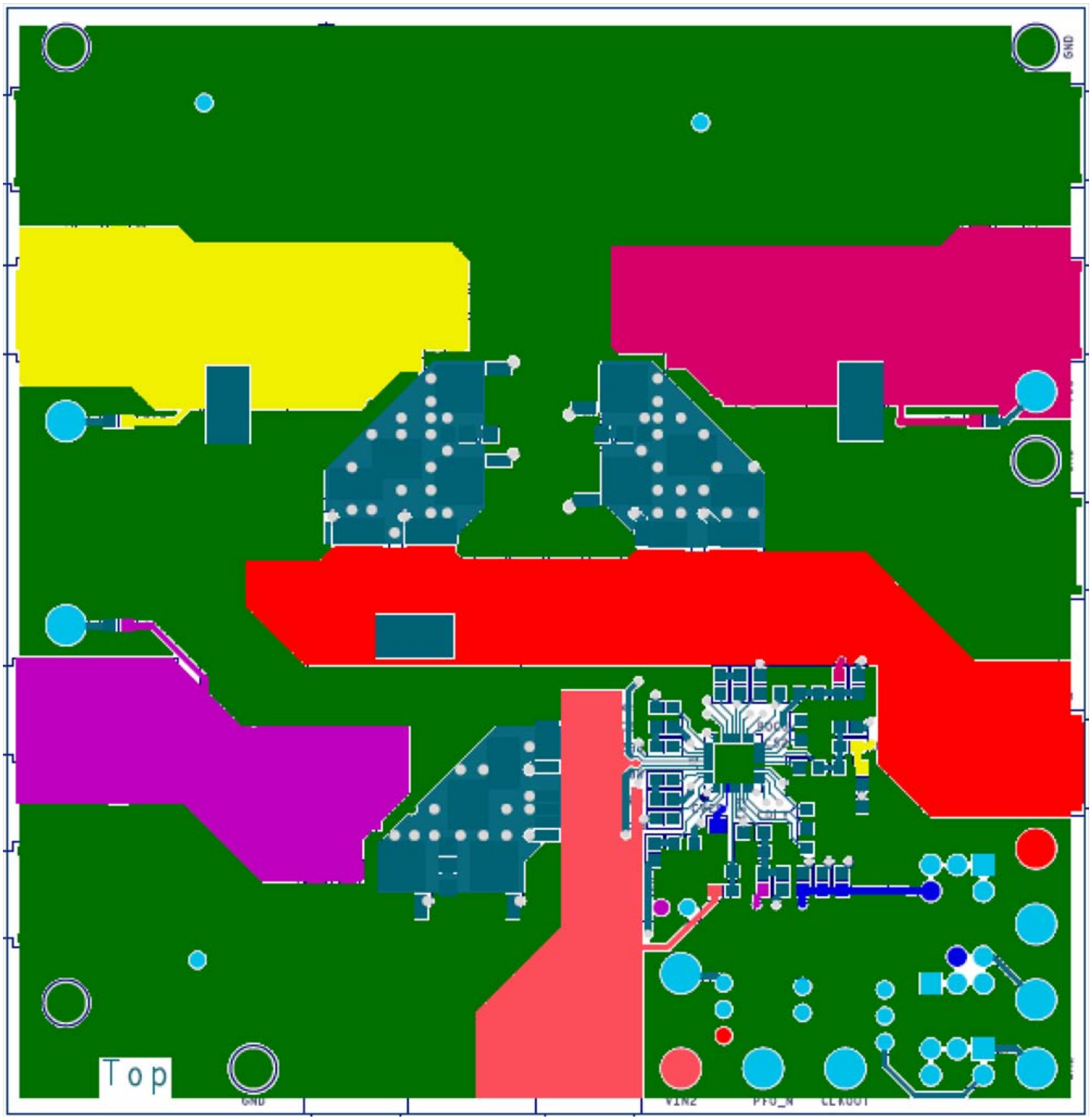


FIGURE 20. TOP LAYER

ISL9444EVAL3Z PCB Layout (Continued)

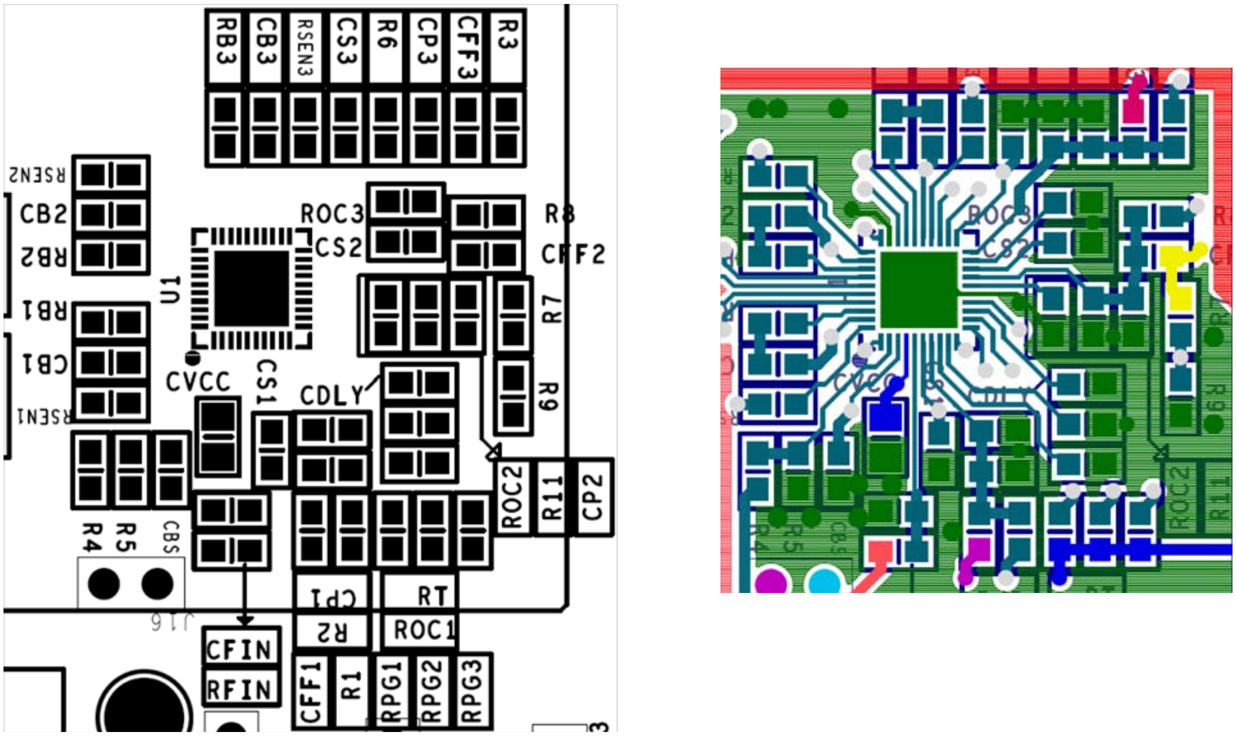


FIGURE 21. TOP LAYER ZOOM IN

ISL9444EVAL3Z PCB Layout (Continued)

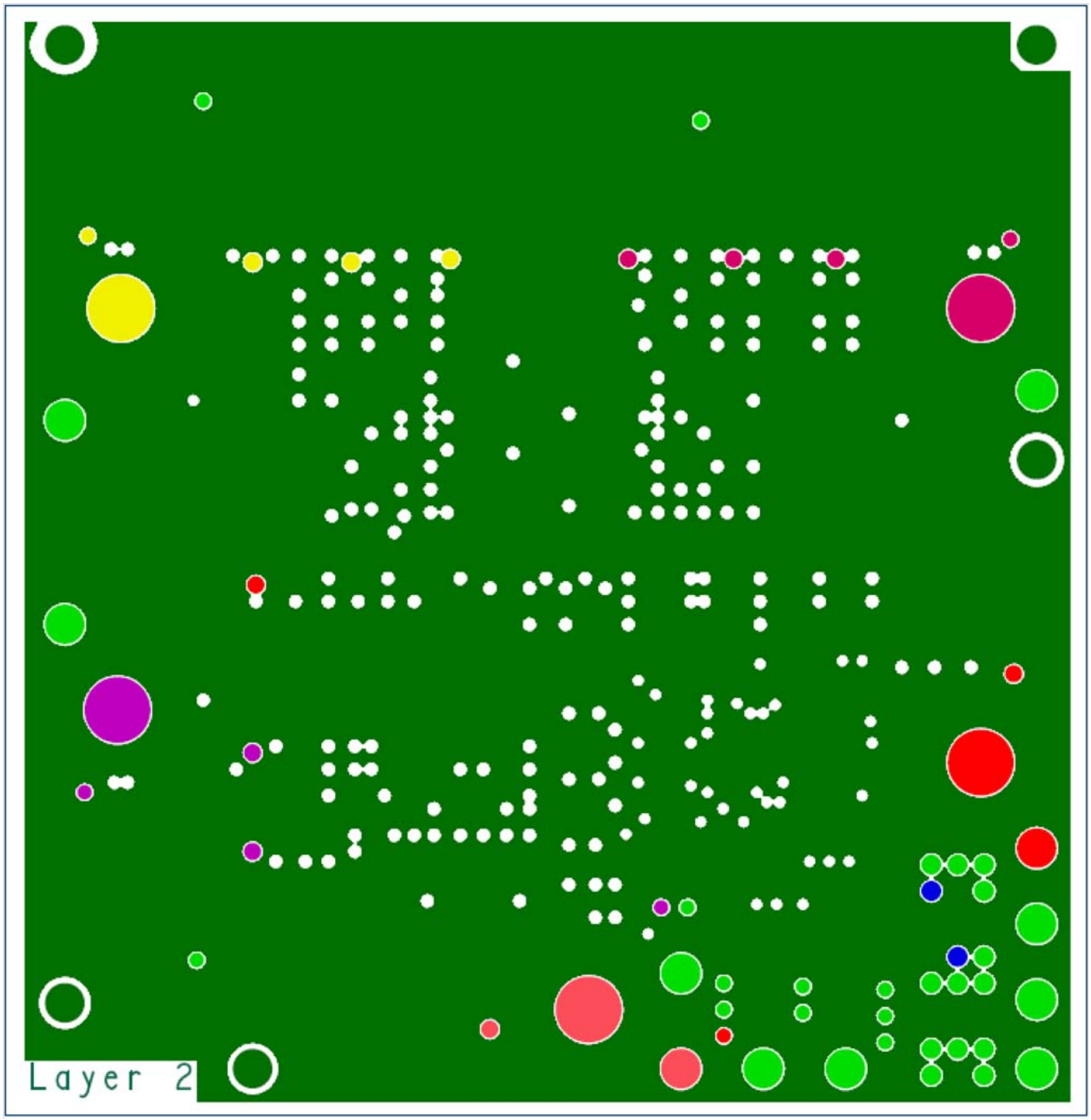


FIGURE 22. SECOND LAYER

ISL9444EVAL3Z PCB Layout (Continued)

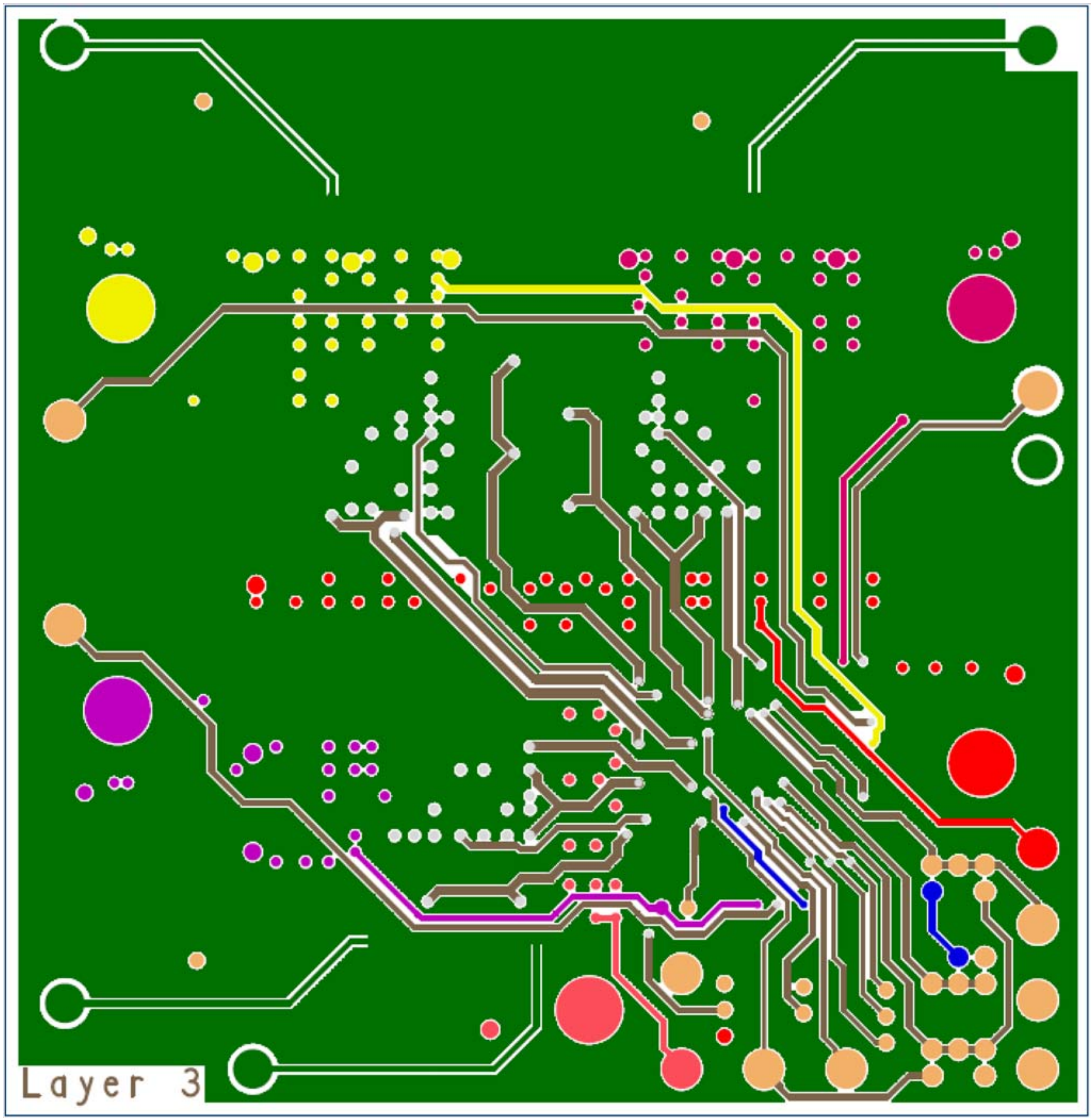


FIGURE 23. BOTTOM SILKSCREEN

ISL9444EVAL3Z PCB Layout (Continued)

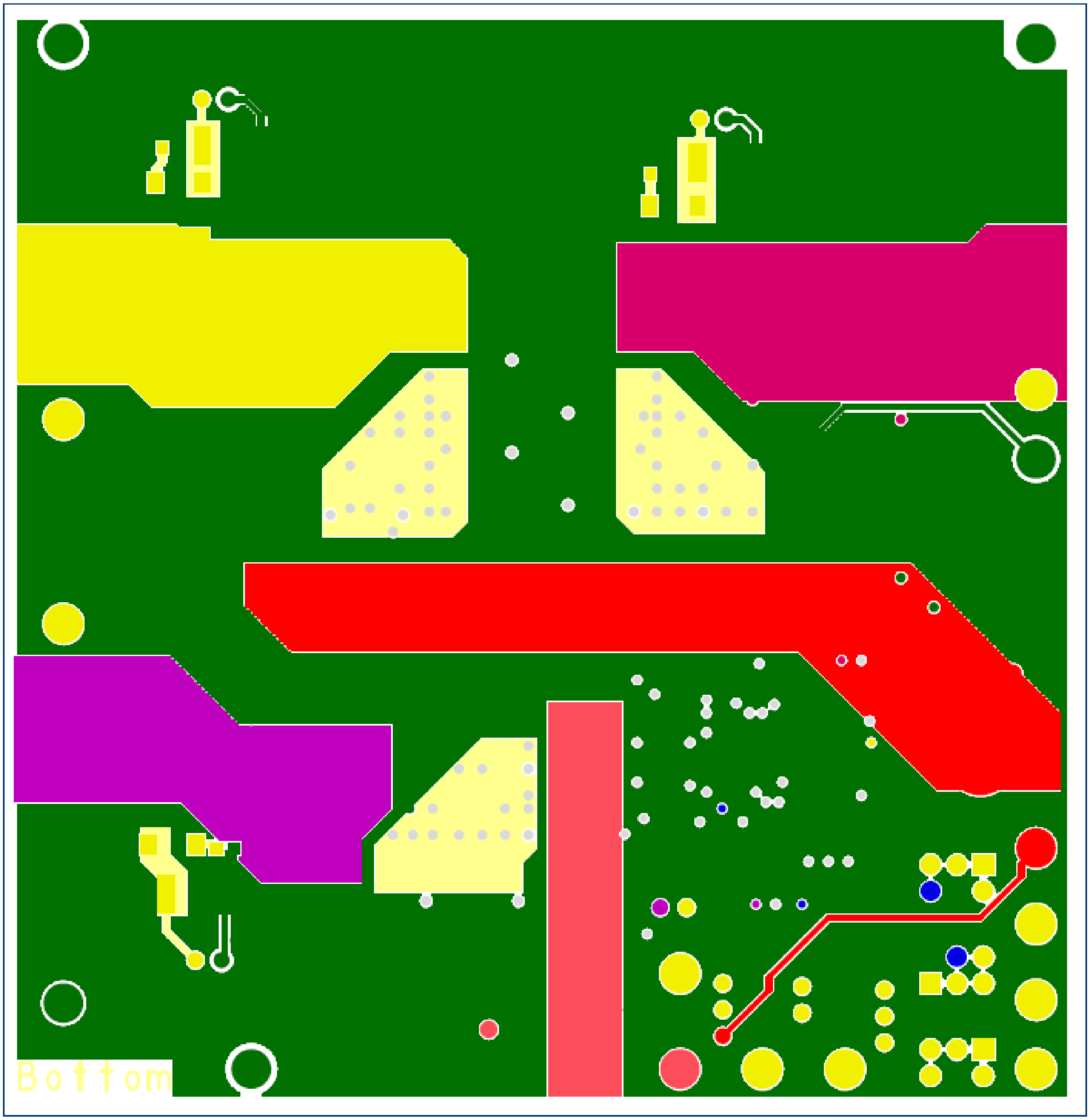


FIGURE 24.

ISL9444EVAL3Z PCB Layout (Continued)

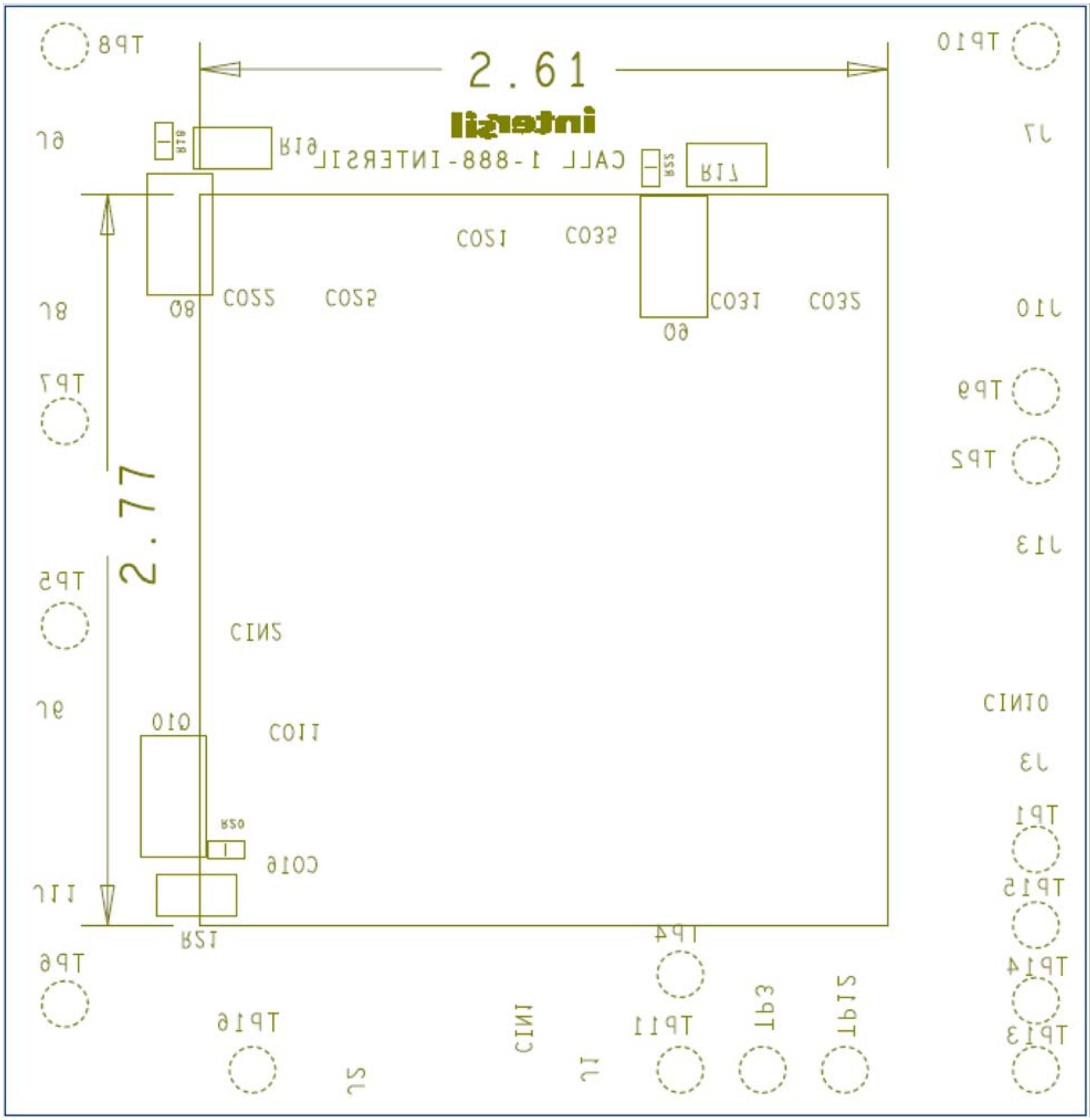


FIGURE 25. BOTTOM SILKSCREEN